



Remarks

Applicants respectfully request reconsideration of this application as amended. Claims 1, 6, 8 and 16-23 have been amended. No claims have been cancelled. Claim 24 has been added. Therefore, claims 1-24 are presented for examination. In the Office Action, the title was objected to. Applicants have amended the title to be more indicative of the invention.

Claims 1-3, and 8-23 stand rejected under 35 U.S.C. §102(e) as being anticipated by Hetherington et al. (U.S. Patent No. 5,978,864). Applicants submit that the present claims are patentable over Hetherington.

Hetherington discloses a system and method for thermal overload detection and protection for an integrated circuit processor. The system allows the processor to run at near maximum potential for the vast majority of its execution life. This is effectuated by the provision of circuitry to detect when the processor has exceeded its thermal thresholds and which then causes the processor to automatically reduce the clock rate to a fraction of the nominal clock while execution continues. When the thermal condition has stabilized, the clock may be raised in a stepwise fashion back to the nominal clock rate. See Hetherington at col. 3, ll. 53-65.

Moreover, the system discloses a thermal sensing circuit that incorporates a programmable threshold which, when reached, causes the circuit to generate a non-masked interrupt to the processor which may be identical to a power down "Energy Star" interrupt. The internal phase-locked loop ("PLL") clock dividers may be employed to step down the master clock from nominal to, for example, 1/64^{sup.th} of the nominal rate. Program execution would then continue at this lowered or reduced clock rate until the thermal sensing circuit again senses that a temperature threshold has been crossed, whereupon it may again issue a non-masked interrupt to raise the clock back to nominal frequency. As before, normal program execution commences at the conclusion of the interrupt (col. 4, ll. 42-58).

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Claim 1 of the present application recites power management logic to enable a CPU to operate in a first execution mode whenever the temperature of the CPU exceeds a predetermined threshold and to operate in a second execution mode whenever the temperature of the CPU is below the predetermined threshold, wherein the CPU executes a first quantity of instructions per cycle in the first execution mode and executes a second quantity of instructions per cycle in the second execution mode. Applicants submit that Hetherington does not disclose a CPU executing a first quantity of instructions per cycle in a first execution mode and executing a second quantity of instructions per cycle in a second execution mode. Therefore, the present claims are patentable over Hetherington.

Claims 2-7 depend from claim 1 and include additional limitations. Therefore, claims 2-7 are also patentable over Hetherington.

Claim 8 recites transitioning from a first execution mode to a second execution mode, wherein the CPU executes a first quantity of instructions per cycle in the first execution mode and executes a second quantity of instructions per cycle in the second execution mode. Therefore, for the reasons described above with respect to claim 1, claim 8 is also patentable over Hetherington. Since claims 9-15 depend from claim 8 and include additional limitations, claims 9-15 are also patentable over Hetherington.

Claim 16 recites an instruction execution unit to generate a first quantity of instructions per cycle in a first execution mode whenever a thermal sensor measures temperature exceeding a predetermined threshold and to generate a second quantity of instructions per cycle in a second execution mode whenever the thermal sensor measures temperature below the predetermined threshold. Thus, for the reasons described above with respect to claim 1, claim 16 is also patentable over Hetherington. Since claims 17-19 depend from claim 16 and include additional limitations, claims 17-19 are also patentable over Hetherington.

Claim 20 recites an instruction execution unit to generate a first quantity of instructions per cycle in a first execution mode whenever a thermal sensor measures

temperature exceeding a predetermined threshold and to generate a second quantity of instructions per cycle in a second execution mode whenever the thermal sensor measures temperature below the predetermined threshold. Accordingly, for the reasons described above with respect to claim 1, claim 20 is also patentable over Hetherington. Since claims 21-24 depend from claim 20 and include additional limitations, claims 21-24 are also patentable over Hetherington.

Claims 4-7 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hetherington et al. in view of McFarland et al. (U.S. Patent No. 5,125,093). Applicants submit that the present claims are patentable over Hetherington even in view of McFarland.

McFarland discloses a technique of servicing interrupts among a plurality of microprocessors. See McFarland at Abstract. Nevertheless, McFarland does not disclose or suggest a CPU executing a first quantity of instructions per cycle in a first execution mode and executes a second quantity of instructions per cycle in a second execution mode. As discussed above, Hetherington does not disclose such a limitation. Therefore, any combination of Hetherington and McFarland would also not disclose or suggest a CPU executing a first quantity of instructions per cycle in a first execution mode and executes a second quantity of instructions per cycle in a second execution mode. Accordingly, the present claims are patentable over Hetherington in view of McFarland.

Applicants respectfully submit that the rejections have been overcome, and that the claims are in condition for allowance. Accordingly, applicants respectfully request the rejections be withdrawn and the claims be allowed.


The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: May 30, 2003



Mark L. Watson
Reg. No. 46,322

12400 Wilshire Boulevard
7th Floor
Los Angeles, California 90025-1026
(303) 740-1980